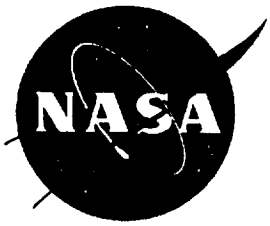
August 25, 1998



USE OF SX SERIES DEVICES

AND

IEEE 1149.1 JTAG CIRCUITRY

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1.0 BACKGROUND AND SUMMARY

This report summarizes the use of SX series devices and their JTAG 1149.1 circuitry. 'JTAG' circuitry was originally designed to standardize testing of boards via a simple control port interface electrically without having to use devices such as a bed of nails tester. JTAG is also used for other functions such as executing built-in-test sequences, identifying devices, or, through custom instructions, other functions designed in by the chip designer. The JTAG circuitry is designed for test only; it has no functional use in the integrated circuit during normal operations.

The JTAG circuitry and the mode of the device is controlled by a circuit block known as the 'TAP controller,' which is a sixteen-state state machine along with various registers. The controller is normally in an operational state known as TEST-LOGIC-RESET. In this state, the device is held in a fully functional, operational mode. However, a Single Event Upset (SEU) may remove the TAP controller from this state, causing a loss of control of the integrated circuit, unless certain precautions are taken, such as grounding the optional JTAG TRST signal.

This application note will cover three devices:

RT54SX16-CQ256BXB45	no TRST signal implemented, internal POR
RT54SX16-CQ256B	external TRST, no internal POR
RT54SX16S-CQ256B	external TRST and internal POR

Each of these three devices must be treated in a unique fashion and understood for proper application.

2.0 IEEE 1149.1 JTAG

2.1 Review of the Specification and Effects

The JTAG specification is defined by the IEEE in Reference 1; a good introduction is given in Reference 2. Please consult these for a more detailed explanation and further background. An overview of the test concept is shown in Figure 1, below, where the core logic of the device is surrounded by a set of scan cells.

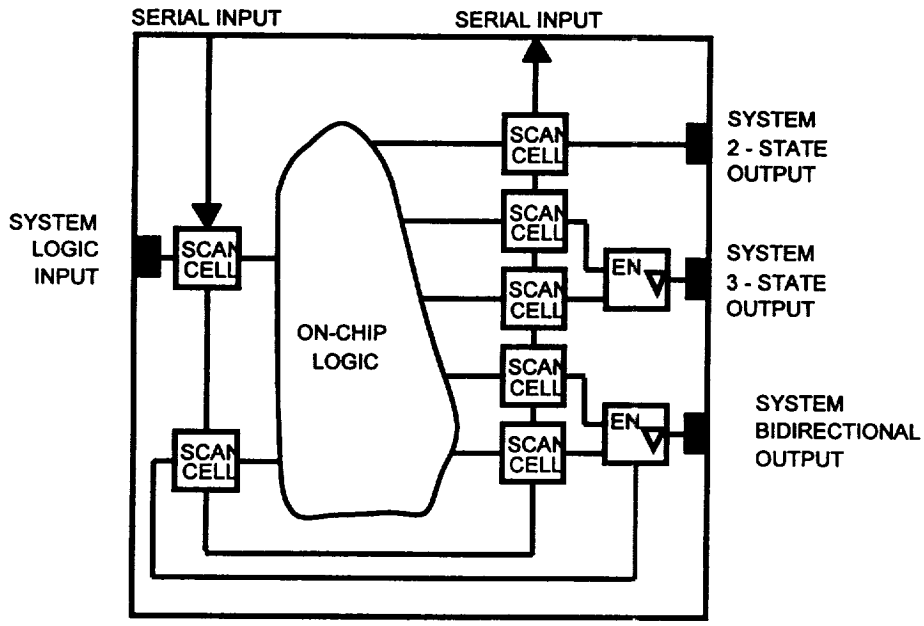

Figure 1: An Overview of the JTAG Scan Path

Each of the scan cells is linked into a shift register and multiple devices on a board are linked together in a serial fashion. A detailed look at a scan cell is shown in Figure 2, below.

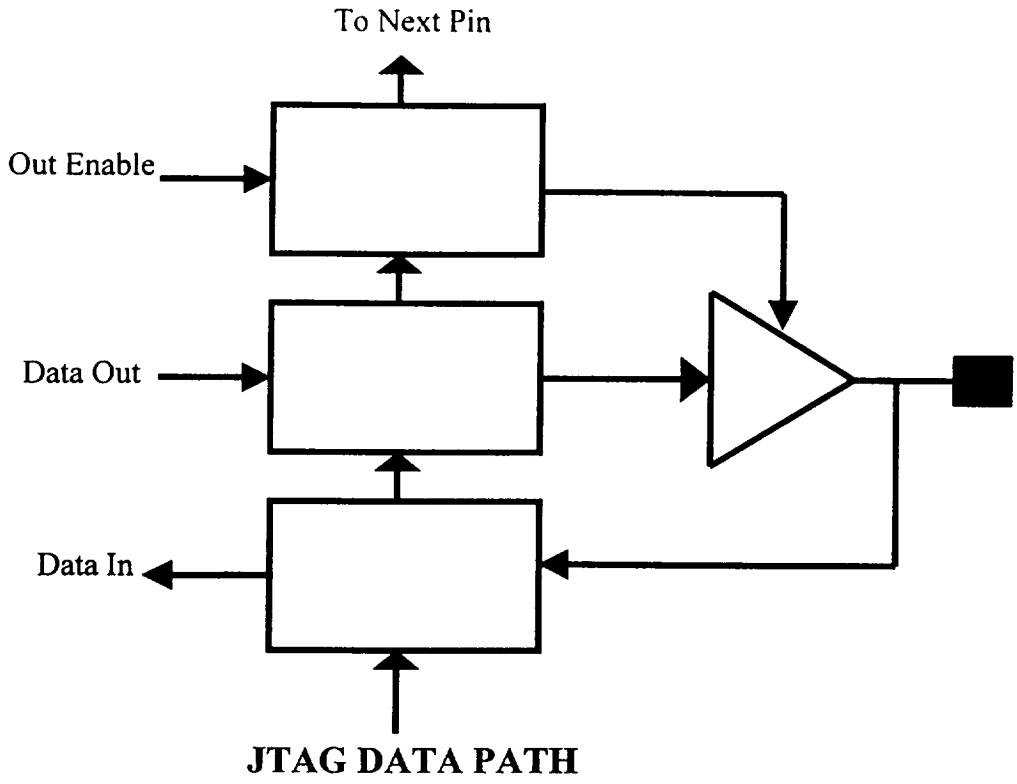

Figure 2. JTAG Scan Cell

Depending on the configuration of the chip and the values in the shift registers, the device I/O's can either function normally or provide a variety of test functions. Examples include sampling external data from the board and 'capturing' it, driving test equipment specified values onto the board, or to place specific values into the core circuitry for test. Other possibilities include capturing a devices outputs, reading special registers, programming, or other device specific functions.

As can easily be seen, many problems can arise from a loss of control. FPGA device inputs can be turned into outputs causing driver contention; board inputs can be blocked isolating the device core; various internal device resources can be configured improperly, etc.

The TAP Controller controls the chip mode as well as shifting data into various registers. The most important register is the Instruction Register which consists of two halves; one half is for shifting in new data and the other is for latching the new command. This is shown in Figure 3, below.

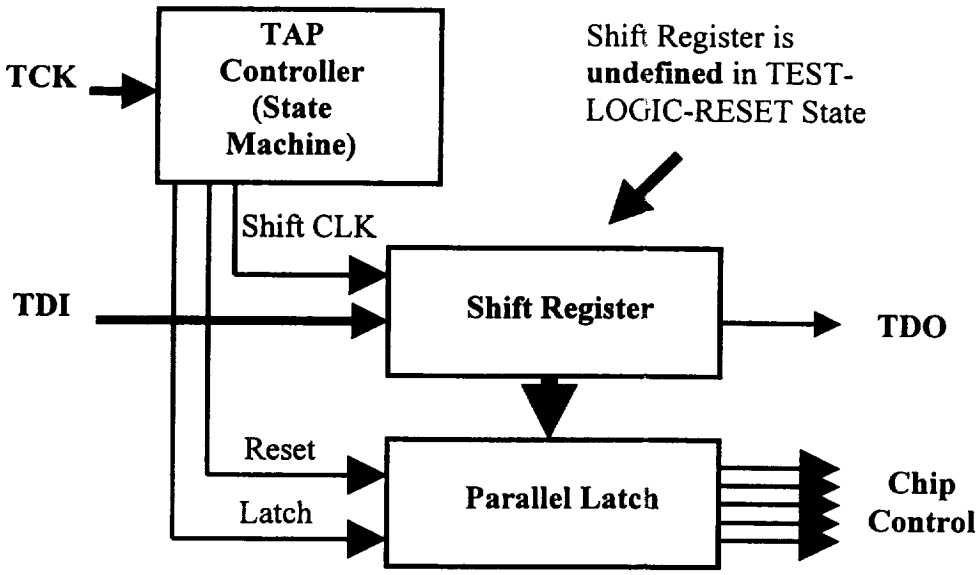

Figure 3: TAP Controller and Instruction Register

As can be seen from Figure 3, the instruction register is loaded from TDI (test data input) and is latched under command from the TAP controller. When the TAP controller is in the TEST-LOGIC-RESET state, the parallel latch, whose outputs control the chip, are asynchronously held in an operational state, independent of values stored in other data registers. This is similar to the function of grounding the MODE pin in the Actel ACT 1, ACT 2 and ACT 3 architectures.

It is critical to note that the state of the shift register is undefined in many of the TAP controller states and is not controlled by Reset. The contents of the shift register can be random values from the power-on condition or may be altered by SEU's. If the TAP controller passes through the IR-Update (instruction register update) state, then the contents of the shift register will be jam loaded into the parallel latch with generally unpredictable results.

A brief examination of the operation of the TAP controller's state machine will show the effects of radiation on this circuitry and how the effects can be mitigated. First, note that three signals control the TAP controller: TMS (test mode select), TCK (test clock), and TRST (test reset), with the last signal being optional. The state machine is shown below:

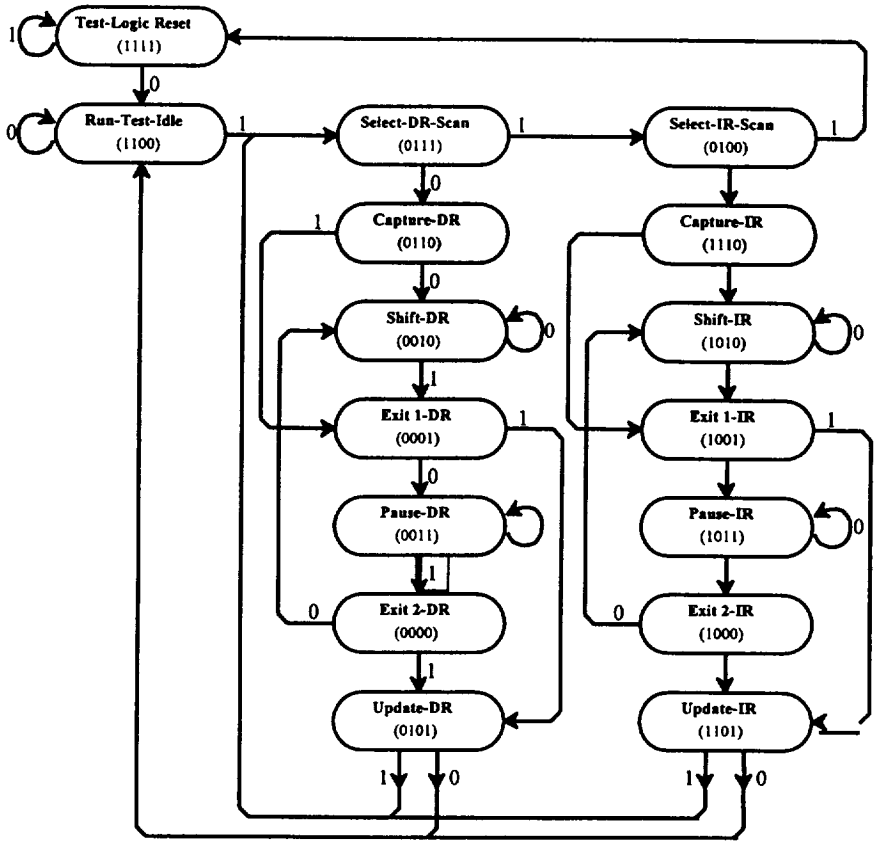

Figure 4:TAP Controller State Diagram

In Figure 4 the value of TMS is shown on the state transitions. Note that the state machine will return to the TEST-LOGIC-RESET state in no more than five clock cycles if TMS is held high, the normal configuration. There are two other ways of entering or maintaining the TEST-LOGIC-RESET state. The first is by holding the TRST signal to ground. The second is by a power-on-reset signal derived in the integrated circuit. Both of these latter two mechanisms may or may not be present. If both of these signals are present, then they are logically OR'd. Different members of the SX series of devices have different configurations. Also, an antifuse may disable the TAP controller in the DX series; this is not available in the SX architecture.

As can be seen from Figure 4, the TAP controller is quite robust to *expected* faults. For instance, an indefinite short to ground on TMS and then removal will not alter the state of the chip. However, it is easily seen that with this state encoding, a single bit fault, from an event such as an SEU, can cause the TAP controller to move from the TEST-LOGIC-RESET state through the following set of transitions: TEST-LOGIC-RESET → CAPTURE-IR → EXIT-1-IR → UPDATE-IR → SELECT-DR-SCAN → SELECT-IR-SCAN → TEST-LOGIC-RESET. When the TAP controller passes through the UPDATE-IR state, the Instruction Register latches the contents of the shift register, whose contents are not controlled, changing the chip's mode.

Data taken during heavy ion testing shows some examples of device configuration errors. Figure 5, below, shows the device shutting down, with the inputs effectively disabled, and the device drawing static power. Beneath that, Figure 6 shows the device drawing large currents; in some runs, currents exceeding 800 mA were observed.

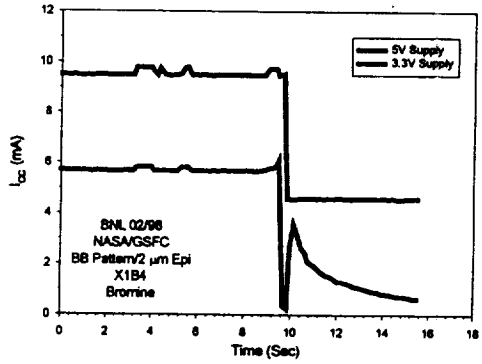

Figure 5: SX Prototype 'Shutting Down' During Heavy Ion Test

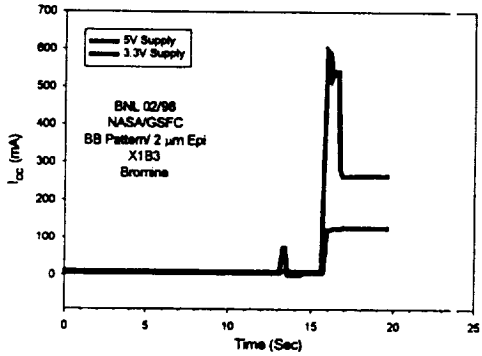

Figure 6: SX Prototype Showing a High Current Mode During Heavy Ion Test

3.0 DESIGN RECOMMENDATIONS

3.1 GENERAL RECOMMENDATIONS AND OVERVIEW

There are three model types currently planned for the RTSX series. For the 'SX16' they are summarized, with respect to JTAG, as follows:

1. RT54SX16-CQ256BXB45 no TRST signal implemented, internal POR
2. RT54SX16-CQ256B external TRST, no internal POR
3. RT54SX16S-CQ256B external TRST and internal POR

Each of these configurations needs to be understood for proper operation of the device. As a general note, the SX series may have the JTAG inputs disabled (normal I/O operation) or enabled, where they have JTAG functionality. This can be controlled by the 'P-Fuse' and should be programmed for the JTAG inputs to be active and the mitigation techniques here to function properly. After programming and installation on the board, the device's configuration can be verified by the presence of an internal pull-up resistor of approximately 10 kΩ on the TMS pin when in JTAG mode. By grounding this pin, an appropriate increase in I_{CC} should be observed.

3.2 RT54SX16-CQ256BXB45

In this model, the TRST signal is not implemented and the TAP controller is initialized and sent to the TEST-LOGIC-RESET state when power is applied by an internal Power-On-Reset circuit. It is important that the power supply rise within the specified time and with an appropriate waveform. Since the TAP controller can be upset, the TCK pin should be connected to a free running clock (up to 20 MHz) and the TMS pin held high. This will minimize the time that the device's configuration is in error.

Heavy ion test data, while not a guarantee, shows the device losing configuration and then returning to an operational state. Figure 7, below, shows jumps in the error counters when the TAP controller is upset by a heavy ion. The JTAG cross-section, while not yet accurately measured, is relatively small, on the order of 10^{-6} cm^2/device, making the probability of a failure on-orbit low, but not zero.

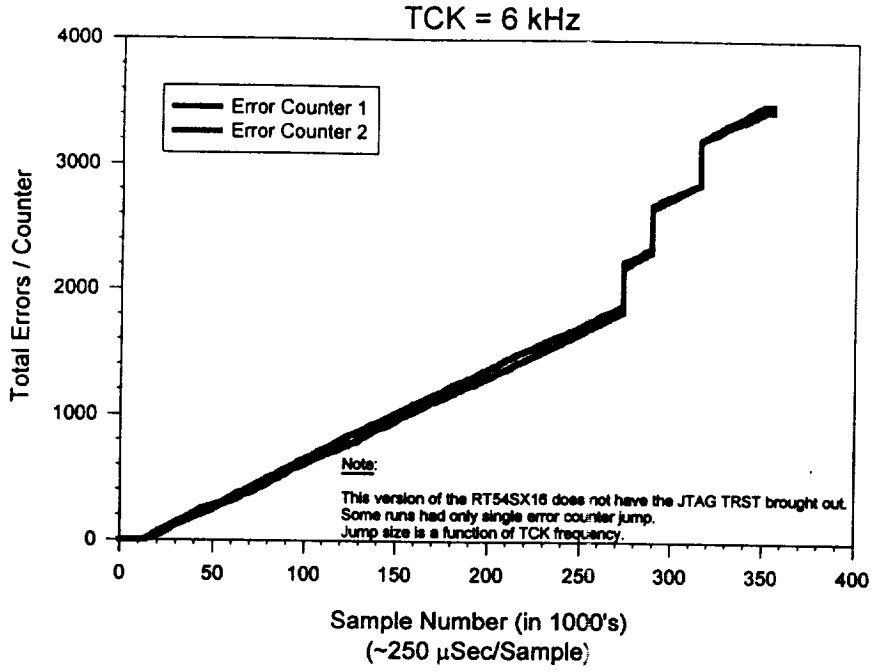

Figure 7: JTAG Upset and Recovery with Heavy Ions at TCK = 6 kHz

3.3 RT54SX16-CQ256B

In this model, there is an external TRST pin but no internal POR signal. It is imperative that the TRST be grounded and verified prior to the application of power to the device, otherwise the device can be powered in an illegal configuration. It is noted that large currents can be drawn in an illegal configuration, exceeding 800 mA, with an unknown impact to device reliability. Properly configured, this device will be immune to any JTAG upsets, since the TAP controller will by held directly in the TEST-LOGIC-RESET state.

Note that verifying that the TRST pin is grounded is extremely important as the JTAG 1149.1 specification requires that an unconnected TRST be pulled high which will prevent the TAP controller from being reset.

3.4 RT54SX16S-CQ256B

In this model, there is both an external TRST pin and an internal POR signal. This permits both an SEU-hard TAP controller for flight and worry-free use of the JTAG port for ground test. The device will, independent of the state of the TRST pin, power up into an operational configuration. If TRST is held high during power-up, a proper V_{CC} rise time and waveform is required. JTAG test equipment can be connected to the device for functions such as observing internal nets.

For flight, it is imperative that the TRST be grounded and verified. In this configuration, this device will be immune to any JTAG upsets in flight, since the TAP controller will by held directly in the TEST-LOGIC-RESET state.

4.0 REFERENCES

1. **IEEE Standard Test Access Port and Boundary-Scan Architecture,** IEEE Std. 1149.1-1990 (Includes IEEE Std 1149.1a-1993), IEEE, October 21, 1993.

2. **Scan Tutorial Handbook Volume I,** National Semiconductor and Teradyne, 1994 Edition.

5.0 Acknowledgements

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